Virtual Video-Sensitive Interface Used in Robotic Control

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ABSTRACT: The paper presents a video-sensitive virtual interface used in technological process controlling. The control panels are substituted by this graphical system, with all advantages that can be focused from there. In robotic control are involved many controlling instruments and whole this set can be implemented with some virtual controls such as below description. Into complete application of robotic control system is necessary a hardware structure coupled on the PC's parallel or serial port which assures the bi-directional information transfer. This

KEYWORDS: Robotics, Interface, Programming Language, Image, Virtual, Microcontroller, Sensitive.

1. INTRODUCTION

An interface is defined as an adaptive system in concordance with the controlled technical process requests and the controlling subsystem. The classical interfaces most often are the hardware structures. Some structures involve specific disadvantages like as:

- high cost (production, maintenance, transport etc.);
- low reliability and physical wear in time;
- high environment factors sensibility;
- high mechanic and electric inertia;
- low up-grade capability.

All this disadvantages can be eliminate by total change between classical interfaces and virtual interfaces.
A virtual interface is an example of primordial software structure, where the hardware is an insignificant part.
This paper is focused to show, like as man-machine interfacing solution, an unusual virtual interface type: the video sensitive interface.
The graphical interfaces are involved where the man-machine interface must be optimized [3]. These interface type outcomes virtual as time as modeling the physical-inertial structures, using by their unsubstantial feature. In this mode a graphical interface has some qualitative characteristics, not proper for other interfaces: non-inertial mechanical or transitional behavior, not wear phenomena, high reliability level, developing and adapting ability to the change systemic requests, low costs etc.
The video sensitive interfaces become from the graphical interface class. One same interface use a combination between a real image which is captured in live mode by video camera (a person's image) and other graphical image which is synthesized by the computational system (some buttons for example). The interaction between the two images is coordinating on-line by the involved person. Thus, in virtual mode, is possible to press a key like as simple gesture in the air.

2. SOFTWARE ENVIRONMENT

The software environment, which was selected, is C++Builder. The choice was be made for speculate the advantages involved by this software environment. Thus, the C++Builder is a visual programming environment and has on base the C++ programming language that is considered in actual moment the best programming language for the lower applications. This aspect assures to the system the developing quality. Other reason for C++Builder choice is the easeful management by computer ports (serial and parallel ports). Under C++Builder exist implements specific function's libraries in ports controlling, which are optimized and tested by a lot of users in various applications.
When is necessary to optimize the system from resources implemented (is possible to wish a software system which adapting to more simplify hardware system) can be using the C standard programming language.

3. THE VIRTUAL INTERFACE

Video interface implementation into the live dynamics is easeful performing in C++Builder [2]. The *CapSetVideoArea(VideoArea)* sets the builder component into is made the capture.
The label which will receipts the state information from the driver, is processed by *CapSetInfoLabel(VideoLabel)* function.
The opening of the setting capture source window (the video-camera) is performed by *CapDlgVSource()* function.
The setting format for capture perform is made by *CapDlgVFormat()* function. In present application was opted for the 320x240 TrueColor.
The image processing procedure is based on the contour analyze algorithm. For that in defined first the background like the image layer which not supports position's variation. The dots from the frame which accepts the motionless condition on all time of prescribed analyze (was been considered a 2 seconds time interval), will belong to background class. The rest from layer is considered moving object. In this mode, the person will be identifying periodically with a 2 seconds rate. The contour analyze will be made on the dynamic image (on the person's image). The

Figure 1. Image with sensitive areas

video-sensitive points are considered the graphical buttons (figure 1). For this is first performed a positioning analyze. The coordinates thus determinate will be stored into the witness vector. Next step consists in launch one the periodically analyze routine for the possible coordinates superposing between the dynamic object area (the person) and the video-sensitive areas (graphical buttons). This one state like as identified will conducts to a specific decision in concordance with the button was been pressed.

4. THE COMPLETE INTERFACING SYSTEM

Like a hardware subsystem can be used any electronic interface board coupled to one from the computer's ports or just a system with microcontroller [Mahalu]. Much more is need a video camera coupled to a PC system. In this application was been used a Logitech kind camera.
The whole structure of the video-sensitive virtual interface system is presented in figure 2.

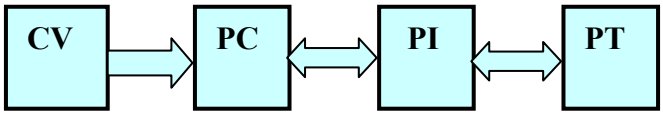

Figure 2. The control system structure

The block notations from figure 2 have the signification:

- video camera VC;
- computer PC;
- interface board IB;
- technological process TP.

The interface board used is DAQ801 type with the follow features:

- 40 ks/s sampling rate;
- 12 bits resolution on the analogue input;
- 8 analogue inputs with simple reference or differentials;
- 2 D/A channels on 12 bits;
- 3 timer/counter on 16 bits;
- 32 digital I/O channels;
- auto-calibration and auto-axing on zero;
- possibility to scanning on the channel with various gain factors;
- FIFO date buffer on 2 kB;
- programmable gain on 1, 10, 100, 1000;
- interrupt management possibilities;
- firm's soft drivers;
- Windows 95/98/NT and Windows 2000 compatibility.

Technical specifications:

Analogue inputs:

Input impedance – 1 MΩ
Voltage protection – up to +20 V
Conversion time – with auto-axing on zero: 25.6 µs, without auto-axing on zero: 15.2 µs
FIFO data buffer – 2K (1024 samples)
Scanning list – 8 inputs
Error on zero – to zero adjusting
Gain error – to zero adjusting
Integral linearity error - ±1 LSB
Noise – in voltage for 1.7 mV_{vv}

Analogue outputs:

Channels – 2
Domain - 0÷5 V , ±5 V
Resolution – 12 bit
Integral linearity error - ±1 LBS
Output impedance – 0.5 Ω
Output current – 2 mA

5. THE RADIO-INTERFACING SYSTEM

A good solution of interfacing performs is to use a radio transmitter-receiver structure coupled by the PC' port. A same structure can be realized using bluetooth technology. However, is possible imagining own communication structure on the high frequency. One same structure is following presented.

6. THE CODING BLOCK

The coding block can be realized in various architectures, in respect with the request imposes to the data sets.

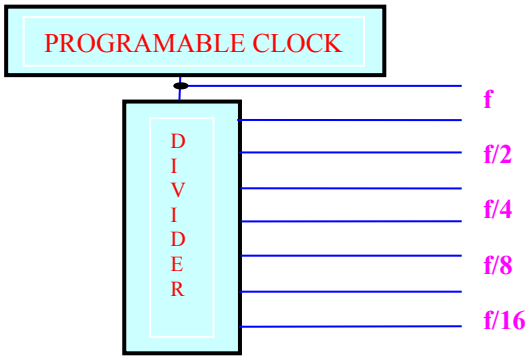

Figure 3. The divider structure

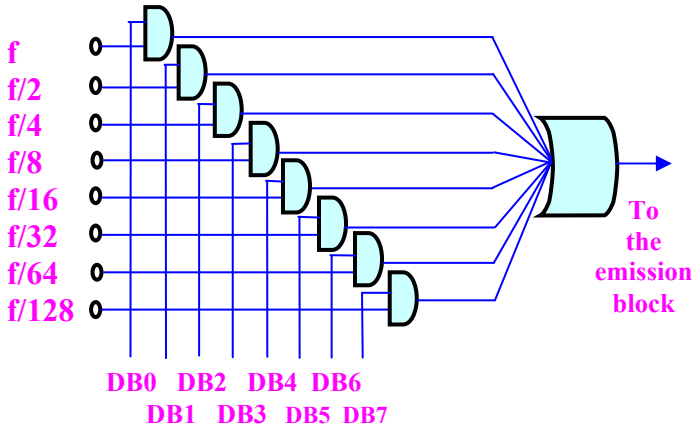

Figure 4. The CLC codifying block

One data coding solution consists in generating by a set the various frequency signals with different commands signification. The easiest way to release a same system is to use a divider clock signal block. Thus, one frequency by one time is emitting and no more another [Mahalu]. This structure is shown in the figure 3.
In the signals multiplexing goal can be used a CLC structure. With this, one single signal is transferred through an AND gate at one time. All the rest of the signals will be inhibits because all other AND gates are disabled. One example of same structure is shown in figure 4.
Another data coding solution using the wide pulse modulation train. This method is able to coding the binary information [Mahalu]. Thus, for the "1" logical value is generated a pulse with the *d1* wide, while for the "0" logical value is generated a pulse with the *d2* wide.
The main advantage of these coding techniques consists in the superior technical performances and in the simplicity. The coding block will be, in this case, useful to designing and implementing and without problem to put to point. The decoding block from the receiver system wills uses by same advantages. The major disadvantage is the law data transfer speed. Indeed, the data transfer speed is in related with the mean between *d1* and *d2* widths. This widths can't be decreased too much because appear the risk to penetrate in the false pulses domain. Same pulses appear from technical causes both to the electromagnetic field level and the electronic circuits of the system implemented level. After the theoretical analysis and the practical tests by some the witness structures we ascertained that the minimal width for the pulses *d1* and/or *d2* most to be up than 100 ms. Is

understanding what for the data transfer speed is the bounded by the unusually low values. The result is that some solutions can be adapted only when the data succeeding speed requests involved by the controlled system are not big. This is the case that involves great time constants, characteristic for the systems with delays.
One codifying block like that above described, using the monostable structures, is shown in the figure 5.

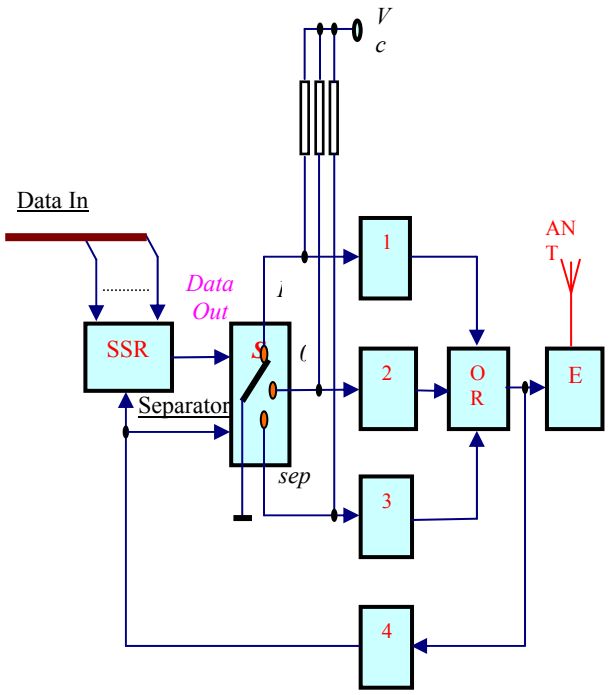

Figure 5. The coding structure

7. DESCRIPTION OF THE WORKING SYSTEM

The *SR* register is with the parallel input and serial output. When is applied a pulse on the *STEP* input in the *DATA-OUT* output appears the next binary value that was loaded in the register. After *N* pulses in the *STEP* input applied, with *N* the *SR*'s register dimension, all the stored bits in *SR* register are obtained in the serial output. The first *STEP* pulse that is provided by the tact formatter-generator, immediately after that is obtained in the *DATA-OUT* output of the last bit stored in the *SR* register, will triggering the loading parallel process. This process will be completed with the extraction in the serial output of the register of the first bit from the new set by the bits was been stored (we refer to most significant bit). The current bit, which is obtained in the DATA-OUT output, is applied by the *SW* switch command input. This switching one by outputs denoted by *1* and *2* respectively in "*0*" logical. Since the outputs are connected each by the monostable input, after the *OR* logical gate will obtain one pulse with *d1* or *d2* about what the bit from *DATA-OUT* was "*1*" or "*0*" logical value. This pulse commands the transmitter circuit denoted by *E*, which will emit a frequency modulation signal with the *d1* or *d2* width. Same pulse provided by the *OR*'s gate will triggering the *M* monostable which will commands the shifting to right with one step of the information contained into *SR* register, with a τ delay.
Another possible solution is that used the *UM 3758-120A* specialized integrated circuit (see figure 6). This chip provides a width modulated pulses train, in relation with the electric states of those twelve inputs, from *A0* to *A11*. These physically inputs can be coupled to *+12V*, to ground or just lets to air. In that mode is possible to generate *531441* distinctly codes. In figure 2 is shown an example of using that circuit for generating two codes. This structure uses *A11* and *A12* inputs. When the *S1* and *S2* push-button are pressed is obtained in Tx output the corresponding pulses train for the codes. The *C1* and *R1* components impose the working frequency for the synchronization oscillator from the coding block circuit.

8. COUPLER WITH THE PARALLEL PORT

The coupling with the parallel port uses an 8-bit buffer that performed so safe separations between the PC port and the adjacent electronics structure. For this buffer can be used specialized logical circuits or just some simple buffers with high impedance outputs. One same block is presented in figure 5. The write mode output signals of this buffer are coupled to the shift register with the parallel inputs and the serial output, in the second case of codify example. For that is possible to be used the 4021 circuit for example [Franklin]. Anyway, in accompany all these will be necessary to be involved a logical control block that processing the state signals from the parallel port. This block will performed too some specific signals designed to the rest of the electronic board interface.

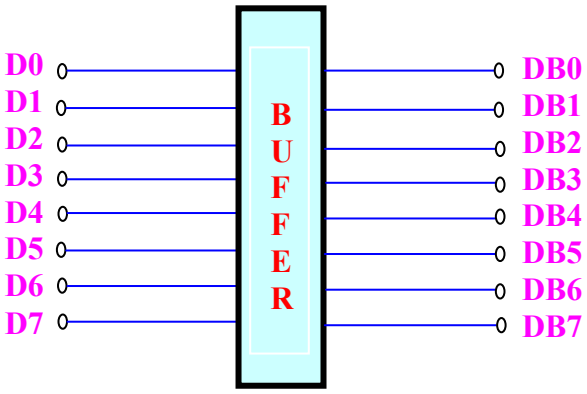

Figure 6. The buffer interfacing with PC port

9. RECEIVER STRUCTURE

In receiver block, the command signal is decoding and only one by *8* output signal lines will be active in *1* logical state, if is working with the CLC codifying block (see figure 5). For to decode a command coded like above is necessary to use a binary counter circuit. This circuit count up just a specified time (called validation time) and function of the frequency command signal the number which result after ending of the counting is more big or more small [Franklin]. All the outputs of the counter circuit constitute an 8-bit bus and this is coupled in sequence to a binary decode circuit. In this mode only one output by the binary decode circuit is activated one time. In figure 7 it shown the described structure.

For remark, whole that structure is used when the coding block generates like signals different frequencies. When width coded pulses are generated, still can be used this structure if a decoder width-time block is used between the receptor block and the counter. One that decoder block is possible to be building with the structures which involves monostable circuits.

When the system contains the UM 3758-120A chip, the decoding block is more simplified because the chip above named can be used like decoder too. In this case the input signal is applied into *Rx* circuit's input and the output consists in the *Tx* signal of the chip. The *Tx* output is a zero logical state while on the transmitter board is pushed the command button. Just is possible to be used more one chips, with the inputs parallel coupled and the distinctly outputs dedicated to the specifics channels. However, in one this case are more necessary some auxiliary blocks, such as logical gates, flip-flop circuits and operational amplifiers.

10. INTERFACING WITH THE PC SYSTEM

When is wished the performing an interfacing between the radio-system board and the PC, will be necessary to create some protocol software procedures. Those procedures must be leading the data control signals transfer on the electronic board. The language which implements the communication protocol from the PC system computer can be a high level language such as the C or the FORTH language.

When is used a microcontroller structure, the system is done independently by the PC. This feature can be exploited in many cases that involve the mobility and low cost requests.

A specifically microcontroller type structure is presented in figure 8. Remark that the system is able to achieving the analogue signals and/or the numeric signals too. The system has the own mini-keyboard and the LCD devices.

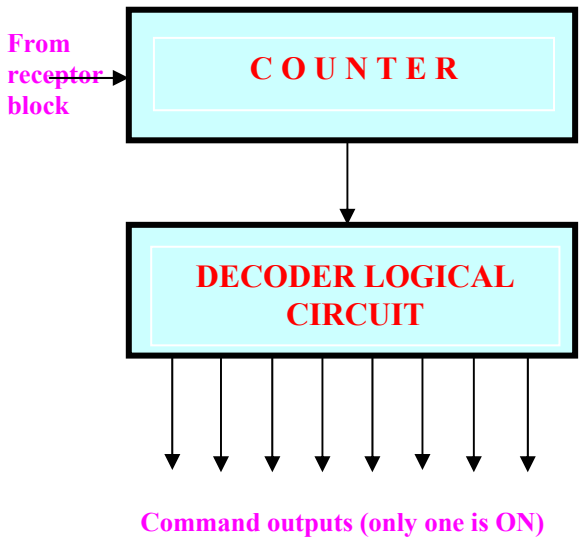

Figure 7. The decoding structure

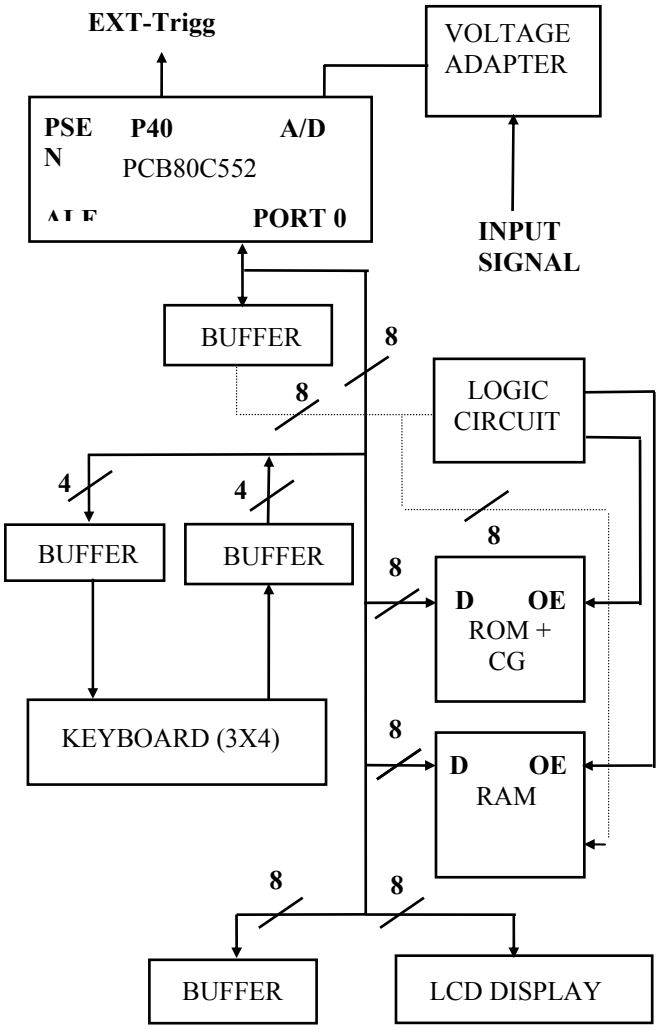

Figure 8. The microcontroller type structure

11. CONCLUSIONS

The developing of software structures and using these more often in the technological processes request implement of the virtual interfaces. These devices become with a set of advantages comparing with the classical interface man-machine, and can conduct to a high quality and economic factors, which are involved into consumption society. The news technologies brings a series of information processing and transfer mechanisms with the specific behavior (like as the Web and Internet technology). The society must be prepared to receiving these technologies and involve them in more knowledge areas.

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